In the Claims:

1-60. (Canceled)

61. (Previously Presented) A semiconductor memory device comprising:

an array of memory cells arranged in an array of rows and columns at a surface of a semiconductor body, each memory cell comprising:

a trench disposed within the semiconductor body;

a conductive material filling at least a lower portion of the trench;

a dielectric material lining sidewalls of the trench such that the conductive material filling the trench forms a first plate of a capacitor and semiconductor material of the semiconductor body forms a second plate of the capacitor, the second plate of the capacitor being electrically coupled to capacitors of other memory cells within the array;

a trench collar lining a portion of a sidewall of the trench above the dielectric material;

a pass transistor having a first source/drain region and a second source/drain region, the first source/drain region being electrically coupled to the conductive material through an opening in the trench collar, the opening formed at one side of the trench such that an asymmetric trench structure is formed;

a plurality of wordlines extending along the rows of the array of memory cells, each wordline being electrically coupled to a gate of every other memory cell along the row;

a plurality of bitlines extending along the columns of the array of memory cells, each bitline being electrically coupled to the second source/drain region of every other memory cell along the column; and

a plurality of isolation regions extending parallel to the plurality of bitlines and disposed between columns of the array of memory cells, each isolation region comprising a rectangular strip of insulating material that extends between adjacent columns of the memory cells, wherein adjacent ones of the memory cells within a column are isolated without use of the isolation regions.

62. (Previously Presented) The device of claim 61, wherein each isolation region has a width and is separated from a parallel isolation by a spacing distance, wherein the width is equal to the spacing distance.

63. (Previously Presented) The device of claim 61, wherein adjacent ones of the trenches are separated by a distance 3F, where F is a minimum feature size.

64. (Previously Presented) The device of claim 61, wherein each pass transistor comprises a vertical transistor.

65. (Previously Presented) The device of claim 61, wherein, for each memory cell, the second source/drain region is located at the surface of the semiconductor body and the first source/drain region is located within the semiconductor body spaced from the surface.

66. (Previously Presented) The device of claim 61, wherein the conductive material filling at least the lower portion of the trench comprises doped polysilicon.

67. (Previously Presented) The device of claim 61, wherein the second plate of the capacitor comprises a doped region of the semiconductor body that extends beneath ones of the trenches.